TRUESTREAM

AXI crossbar

A crossbar is a very common component in an AXI subsystem. Typically in FPGA projects there are more modules/accelerators than there are physical AXI ports. In this case a crossbar is used to perform N-to-1 arbitration of the AXI buses. Since resource utilization is often critical in FPGA projects, Truestream has developed a very efficient IP to perform this operation.

Key features

- Performs N-to-1 arbitration of AXI read and write buses.
- Follows the AXI4 standard.
- Very small logic footprint.
- Achieves 100% utilization of the data channels (R and W) without overhead. The address channels (AR and AW) have a one cycle overhead per burst.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Resource utilization

The design is highly area optimized, while remaining portable. Below is a comparison with a competitor's AXI crossbar implementation, when targeting a Xilinx 7-series device. All the comparisons are done with four buses, i.e. a 4-to-1 arbitration.

Read arbitration, data width 32		
	Truestream	Competitor
LUT	81	289
FF	6	205

Read arbitration, data width 64		
	Truestream	Competitor
LUT	81	367
FF	6	269

Write arbitration, data width 32		
	Truestream	Competitor
LUT	159	340
FF	20	183

Write arbitration, data width 64		
	Truestream	Competitor
LUT	191	376
FF	20	183

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