TRUESTREAM

AXI interconnect

An AXI interconnect is used to connect many AXI masters, that might be of different widths and in different clock domains, to a single physical AXI port. This is typically needed when an FPGA design has more modules/accelerators than physical AXI ports. The interconnect performs N-to-1 arbitration, clock domain crossings and data width conversions as needed.

This interconnect developed by Truestream is unique since it guarantees 100% utilization of the bus in all scenarios. Even if the AXI masters are not well-behaved in an AXI sense, zero cycles will be wasted on the physical port.

Key features

- Compliant with the AXI4 or AXI3 standard.
- Guarantees 100% utilization of the data channels (R and W) without overhead.
- Very small logic footprint.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Performance comparison

The design is highly area optimized, while remaining portable and high performing. Below is a comparison with a competitor's AXI interconnect implementation, when targeting a Xilinx 7-series device. The comparisons are done with four 32-bit AXI masters in a 150 MHz clock domain connected to a 64-bit physical AXI slave port in a 300 MHz clock domain.

AXI read interconnect		
	Truestream	Competitor
LUT	1090	2098
FF	1618	3132
BRAM36	4	4
Bus utilization	100%	85%

AXI write interconnect		
	Truestream	Competitor
LUT	1456	2236
FF	1820	3018
BRAM36	4	4
Bus utilization	100%	85%

The bus utilization figures refer to the utilization of the R/W AXI channels. They are based on a simulated use case where the AXI masters are not well-behaved.

Address
Truestream AB
Brynhilds gata 7
583 72 Vikingstad

Contact
info@truestream.se
www.truestream.se

VAT number
SE559166520201