TRUESTREAM

Off-chip FIFO

An off-chip FIFO, also known as a “virtual FIFO” or “deep FIFO”, is a FIFO structure where data is stored in DDR SDRAM. This is unlike traditional FPGA FIFOs where data is stored in on-chip Block RAM or LUTRAM. This makes it possible to buffer vastly more data compared to the limited on-chip resources.

This off-chip FIFO developed by Truestream uses AXI for off-chip memory transactions. Data in fabric is streamed to and from the FIFO using a simple AXI-Stream-like interface. The IP is uniquely versatile and user-configurable, while maintaining a very small logic footprint.

Key features

- Compliant with the AXI4 or AXI3 standard.
- Each packet length is determined based on the AXI-Stream TLAST signal, not using a static compile-time value.
- There is no lower or upper limit on packet length. The core performs burst splitting and 4k alignment when needed.
- Address range for off-chip memory buffer can be set and updated during runtime.
- Very small logic footprint.

Format

- Written in VHDL-2008. Can be used in any design targeting any vendor.
- Delivery contains human-readable source code, testbenches, and technical documentation.

Resource utilization

The design is highly area optimized, while remaining portable and high performing. Below is a comparison with a competitor’s off-chip FIFO implementation, when targeting a Xilinx 7-series device. The comparison is done with an address width of 28 and a data width of 64.

	Truestream	Competitor
LUT	385	1271
FF	356	1837
BRAM36	2	2.5

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